**Data Sheet** 

## **Product Highlights**

# Application Switch Development Made Easy

- Design business logic in ANSI C
- Optimize and compile the logic to FPGA
- Apply the logic to the raw network streaming data
- Cut development time in half and iteration time by 80%

#### **UDP Reference Design**

- Provides a "pass-through" framework to the network into which proprietary business logic can be inserted
- Full access to the 10 Gbps streams

#### **Analytical Tools**

- Analyze streaming flows of individual modules to optimize I/O
- Use desktop simulation tools such as Visual Studio®
- Use a graphic depiction of code parallelization in hardware to analyze how your code is parallelized
- Reference results of code optimization back to the original C code
- Measure performance in clock cycles using Quartus II Signal Tap II, or the internal debugger, or a VHDL simulator

#### **Tool Flow**

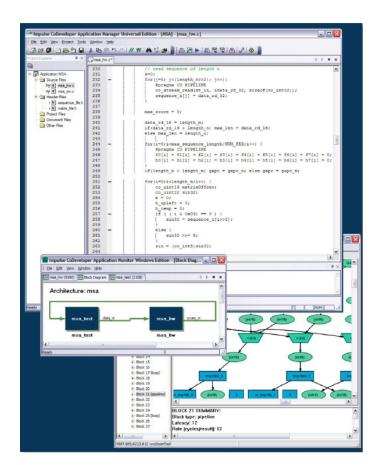
- · Design in ANSI C
- · Simulate on standard C development tools
- Identify opportunities to increase parallelism
- Refactor into coarse grained logic
- Parallelize into multiple streaming processes
- Export to Altera Quartus II (included) to create FPGA programming file
- Download to FPGA via switch CPU or FPGA programming cable

#### Overview

The Arista 7124FX Application Switch is a high performance, ultra-low latency embedded application switch with an inline programmable subsystem that is directly integrated with the switch forwarding plane. The integrated FPGA subsystem provides the unique capability to run latency sensitive and high-throughput mission critical applications directly in the switch, improving performance and determinism while reducing overall latency and footprint.

The Arista 7124FX Application Switch Development Kit provides everything needed to compile and test code on the Arista 7124FX Application Switch.

The 7124FX Application Switch Development Kit includes a complete set of tools specifically designed to enable developers to leverage existing logic and refactor microprocessor targeted C into coarse grained logic suitable for automatic optimization into multiple streaming processes. The kit provides tools for both simulation and stage delay analysis to reduce clock cycles and maximize parallelism, to achieve the lowest possible latency and maximize the performance of the Application Switch. Additionally the kit provides the entire compilation flow for the 7124FX Application Switch FPGA allowing for final code download to the Application Switch FPGA via the Arista EOS operating system, or by directly connecting to the FPGA via the included programming cable.



Impulse Development Tools



## Impulse Platform Library

The 7124FX Application Switch Development Kit adds an Impulse Platform Library for the 7124FX. This library enables the compiled design modules to access hardware elements on the switch. In this manner, the C code can address I/O, memory and other elements without developers having to write specific routines dramatically lowering development time.

FPGA designs are traditionally developed using VHDL or Verilog. Using a higher level language such as C enables developers to port existing C code or create new C applications using standard development tools such as GCC or Visual Studio® and use existing methods for application debugging.

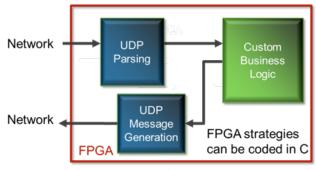
Within Impulse developers experiment with partitioning portions of the C design to run in FPGA hardware or natively in a processor. The C code targeted towards hardware operation is parallelized, then converted to synthesizable HDL. The HDL becomes the input file for the Quartus II software from Altera. Quartus II optimizes the HDL for placement and use of logic resources on the FPGA. The C code targeted towards native operation is compiled to run on the optional soft core processor or can be directed to other processing resources.

# C language applications Generate Generate Generate accelerator hardware software hardware interfaces interfaces C software HDL files **libraries FPGA** device

Impulse Platform Library

# **UDP Reference Design for Financial Services**

The UDP reference design is provided to help development teams quickly experiment with optimization of different algorithms. It basically provides a "bump in the wire" into which teams can insert different filters, trading modules, analytics and other elements of hardware based financial strategies. Systems can be developed which pre-parse incoming messages or execute trades based on custom algorithms or triggers. This can be programmed to parse packets of interest and hand them off to host system user space or programmed to directly act on the data. This method reduces processing variation, decreases latency and offloads the host processor.



UDP Reference Design

Teams can experiment with a complete inbound and outbound trading system to parse data, implement strategies and send outbound messages to the exchange, all from within an FPGA and with no CPU intervention. Hardware based trading systems make ultra-low latency possible by processing data in-line and without an operating system. FPGAs are used to create a customized network interface, handling packets at near wire speed, even in high market conditions. FPGA based trading systems process orders in consistent, deterministic, ultra-low-latency intervals. Software based systems are controlled by operating systems, hardware based systems are not. Operating systems can introduce processing variance (i.e. jitter) during high market conditions. These variations can delay trade completion and raise concerns about successfully executing trading strategies. Hardware based trading systems remove variations and limit uncertainties by reducing or eliminating the role of an operating system.

#### Other IP and Services

Impulse offers intellectual property in FIX/FAST, OPRA and other financial protocols. Impulse also provides several levels of application integration support. In addition to the basic to the UDP reference design, the next level of support is to add a market protocol and a reference design that includes trading logic. These solutions typically include a TCP/IP offload engine. Impulse also provides full custom solutions that can be professionally installed and maintained by Impulse staff.



# 7124FX Development Kit | Ordering Information

## **Development Kit Contents**

- Impulse C annual license
- Impulse C Platform Support Package (PSP) for the 7124FX
- Impulse C UDP Reference Design
- · Altera Quartus II annual license
- Altera IP licenses required for image compilation
- Terasic USB Blaster programming cable
- 15 hours of remote Impulse Factory Engineering assistance or training

## **Development Kit Requirements**

- Windows XP Pro or 7 64-bit
- Intel i7, Xeon, or equivalent
- 16 GBytes memory
- · USB 2.0 interface
- Internet Access

| Product Number  | Product Description   |
|-----------------|---|
| DCS-7124FX-DEV1 | Application Switch development and programming software, programming cable, 15hrs support |

# Service and Support

Support services including next business day and real-time engineering consultation are available. Additional engineering services, training, and custom development may be purchased as required.

# **About Impulse**

Impulse C has been used by over 500 financial, government and industrial teams in the U.S, Europe and Asia. Customers include confidential trading and banking, NASA, JPL, Northrop Grumman, Canon, Toyota, Honda, national security organizations and research universities worldwide. The Impulse tools were originally developed in a U.S. government research lab and were commercialized in 2002. www.ImpulseC.com

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