7130 Developer

FPGA Development & Deployment made easy

The Arista 7130E and L Series devices leverage the latest FPGA technology to enable the development and deployment of cutting-edge network applications. Arista provides a set of mature development kits as well as IPCores to enable firms to build their own applications based on these building blocks.

Arista Development Kits

1. Arista FPGA Development Kit (or Arista FDK)

The Arista FDK provides the documentation, libraries and examples which enable developers to build new FPGA applications running on Arista's 7130 platform. The development environment includes:

- Hardware documentation and information (currently supporting the 7130 E, EH, L and LB development standards)
- IP Cores
- Working example applications, including example build systems
- Support resources to correctly build FPGA applications.

Note: The examples in the Arista FDK target the MOS operating system, and its MOSAPI SDK. As the 7130 Series transitions to EOS, these applications will transition to an enhanced EOS SDK. Please get in touch to discuss your specific SDK feature requirements. EOS application examples will be added in Q4, 2020.

Arista FDK IP Cores Support:

The Arista FDK includes all current Arista IP cores (FPGA libraries). These include:

1. 10G MAC-PHY IP Core: a Ultrascale/Ultrascale+ MACPHY, which is a combined 10GbE/1GbE, low latency design that implements the MAC, PCS & PMA reconciliation layers as four independent channels grouped per the Xilinx transceiver "Quad".

2. Mux IP Core: a Ultrascale+ 10GbE Mux, which is Arista's Low Latency MetaMux Application in an IP Core, with the addition of fabric AXI4 Stream interfaces to inject packets directly from the custom logic.

3. TS IP Core: A clock synchronisation and timestamping core which combines both hardware and software components to synchronise the hardware within 7130 to a PPS, PTP or NTP time source, and use that synchronised clock to measure timestamps.

2. The Arista Switch Development Kit for Vitis™

Vitis is a powerful tool, designed by Xilinx, to better enable FPGA development. Vitis is designed to make it simpler to build FPGA applications using higher-level languages, reusable blocks, and a statically configured Vitis Target Platform in the FPGA. Arista provides support for Vitis development, via these Vitis Target Platforms which run on the LB development standard and support the many Ethernet interfaces provided by the 7130LB devices. The Switch's internal CPU connects via PCIE to the FPGA, and supports XRT, giving a similar development experience to that of a server with an add-in PCIE card.

The Arista Switch Development kit provides:

- MOS support for running Vitis target platforms. Arista's MOS includes Xilinx's XRT and its drivers
- A Vitis target platform for the FPGA in the Arista 7130 LB devices;
- An Arista app for managing the shells installed on a switch;
- An Arista 10GbE Ethernet kernel, including an example application using the Ethernet kernel;
- Example Vitis projects, including Xilinx's Market Maker example, and a software layer used to integrate this into the switch's operating system.

Note: The Arista Vitis Development Kit supports the MOS Operating System. Along with the Arista FDK, support for Arista's EOS will be added in Q4 2020.

Arista 7130 IP Cores

Arista develops FPGA applications based on a mature set of network logic IP and licenses the IP as IP Cores for use on the Arista 7130 platform. These are supported, proven building blocks that reduce the time to implement your applications.

CORE	OVERVIEW	USE IT FOR ...
10G MAC-PHY IP Core	An IP core for interfacing 10 gigabit Ethernet with low latency. • Implements a low latency Ethernet MAC and Physical layer (10GBASE-R) • Connects directly to FPGA top level serial transceiver pins and provides separate AXI4 interfaces for RX and TX user data • Supports Xilinx Virtex® 7, Xilinx Kintex® UltraScale™, and Virtex® UltraScale+™ FPGA's.	• Accelerating your own applications access to the 10G network
Mux IP Core	• Implements the same functionality as the MetaMux application. • Allows for customizable radix and number of multiplexing cores e.g. one 4:1, plus a 13:1, plus a 14:1, etc	• Sharing the FPGA between the mux functionality and your own application • Building a multiplexing app with different configurations than the standard MetaMux application.
MMP IP Core	Provides a bus that leverages parallel I/O between FPGA's on the 7130 triple FPGA platforms. • 8 ns intra FPGA latency • Provides a low latency clock domain crossing FIFO • Supports four MMP links connecting each Leaf FPGA to the Central FPGA and two MMP links connecting the two Leaf FPGAs together	• The lowest latency , parallel communications bus for your multi FPGA applications • The fastest way to involve two FPGAs in a trading decision such as "splitting risk logic from trading logic".

CORE	FEATURES	BENEFITS
Timestamp IP Core (TS IPCore)	Provides a timestamping and synchronisation engine, implemented as a combination of an encrypted RTL core, with a python based synchronisation daemon. When instantiated in a design, the RTL core and software combination allows the system's OCXO to be synchronised to a PPS, PTP or NTP source. Multiple timestamper units can be instantiated to sample asynchronous strobes, providing nanosecond-precise timestamps within the RTL. The TS IP Core solution has the following specifications: • 1ns timestamp resolution with a +/- 2ns precision • Configurable triggering	• Integrating accurate timestamping into your own apps, without having to build and calibrate synchronisation infrastructure. • Utilising precisely synchronised frequencies for Video or other synchronous systems.

Partner Ecosystem

Several tried & tested integrations exist via our technology partners. We enable our partners to deliver value and differentiation in a highly competitive marketplace. Joint innovation with our partners has proven to generate powerful complementary solutions that run on the 7130 platform and offer clients additional capabilities: optimized analytics, data capture solutions, and more.

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